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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,926	11/21/2003	Yuji Takaoka	09792909-5767	3342

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EXAMINER	
BRYANT, DELORIS S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,926	TAKAOKA ET AL.	
	Examiner	Art Unit	
	Deloris Bryant	2813	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response to advisory action dated November 29, 2005 and subsequent RCE filing dated December 12, 2005 is hereby acknowledged.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 17-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger (US 6,159,767) in view of Borwick, III et al (US 2004/0227201) in further view of Nakamura et al (US 2003/0006441). Eichelberger discloses a method of fabrication of a

semiconductor device, comprising the steps of: die bonding of a plurality of semiconductor chips [12] on a substrate [14,Fig. 1]; forming of a first insulation film [16] on said substrate, wherein a top surface and at least a portion of side surfaces of said plurality of semiconductor chips are incrusted in said insulation film [16, see Fig. 1] and wherein each said semiconductor chip is set so as to float on an adhesive resin applied on said substrate (Fig. 1). Eichelberger, however, does not teach forming a target mark in the substrate nor does he teach forming a second or third insulation film whereby the second insulation film is flatly grounded. Eichelberger also does not teach forming a connection hole through the first, second and third insulation film or the forming of wiring on the third insulation film. Borwick, III, however, does teach forming an alignment mark (Fig. 2, 55) in the substrate. Furthermore, Nakamura teaches multiple layers of insulating film (Fig. 1, 11a-d) whereby the insulating film 11c is flattened (pg. 8, para. 0169). Nakamura also teaches forming a connection hole through the insulating film 11a-11d and also the forming of wiring (Fig. 1, 14a-14c) that is electrically connected with the lower region of the semiconductor device (pg. 8, para. 0178). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the method of Eichelberger with the teaching of Borwick, III and Nakamura. One would have been motivated to so modify Eichelberger for the benefit having alignment marks in the substrate to allow for precise vertical alignment of all upper layers of the structure (Borwick, III; pg. 2, para. 0029) and having multiple layers of insulating film with increasing etching selection ratio between each layer to allow the connection hole to be patterned in a controlled manner (Nakamura; pg. 8, para 0171).

Claim 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger in view of Borwick, III et al (US 2004/0227201) and Nakamura et al (US 2003/0006441) in further view of Hudak et al (5,656,552). Eichelberger, Borwick and Nakamura do not teach a substrate comprising a silicon wafer. However, Hudak does teach that a "substrate may be a rigid material such as ceramic or semiconductor". Silicon is a well-known semiconductor used throughout the art. Further Eichelberger, Borwick and Nakamura do not teach the removal of said substrate [Fig. 1]. Hudak, however, does teach the removal of said substrate [Fig. 8-9, col. 7, lns 63-67 and col. 8, lns 1-10]. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to form a multi-chip semiconductor that is substrateless. One would have been motivated to so modify Eichelberger along with the teaching of Borwick, III, Nakamura and Hudak for the benefit of allowing the semiconductor device to have flexibility in any direction [col. 8, line 47].

Response to Arguments

Applicant's arguments with respect to claims 17-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Deloris Bryant whose telephone number is (571) 272-8670. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

dsb

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800